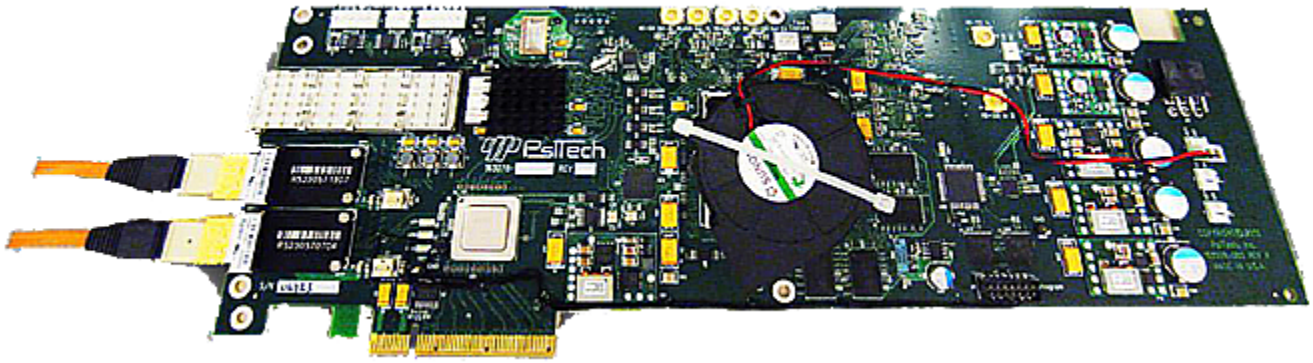
Tornado VR™

Vision Research RTO Interface



Reference Manual

VISION RESEARCH
An AMETEK Company

PN: TBD
Updated: 7/12/2011

Table of Contents

1 Tornado VR Reference Manual

1.1 Introduction

The Tornado VR PCIe board provides high frame rate capture and HD data conversion for high end video camera devices.

Scope

This document provides information for the operation, and driver-level programming of the board.

Purpose

The purpose of this document is to provide enough information to users and developers to give the knowledge necessary to write driver and application interfaces for the Tornado VR PCIe board.

Reference

SMPTE 274M-2003

SMPTE 296M-2001

SMPTE 372M-2002

DS440 Technical documents

Phantom 7.2 Document

NOTE:

When using the Psitech drivers for interfacing with the tornado card the following devices will be available.

WINDOWS

On a windows 7 system the tornado can be accessed through the following devices:

RAM device:

CYVR-RAM (access as \\DosDevices\\CYVR-RAM)

FPGA register device that allows access to the control and status registers:

CYVR-REG

UART devices:

CYVR-COM10

CYVR-COM11

CYVR-COM12

You can read and write these devises to control the Tornado card

LINUX

On a Linux system the tornado card can be accessed through the following devices:

/dev/psi_cyvr_fpga for accessing the control and status registers

/dev/psi_cyvr_ram for accessing the captur buffer ram

UART devices:

/dev/ttyPC0

/dev/ttyPC1

/dev/ttyPC10

or

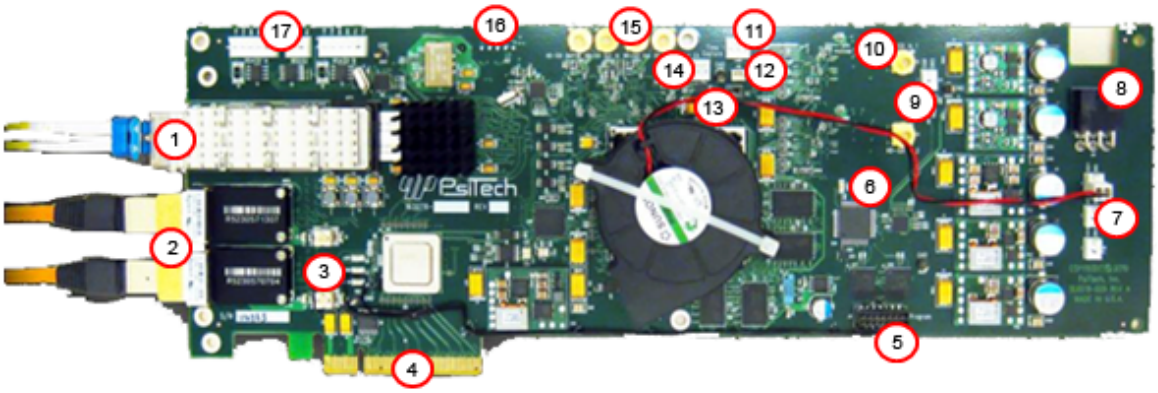
/dev/ttycyvr0

/dev/ttycyvr1

/dev/ ttycyvr2

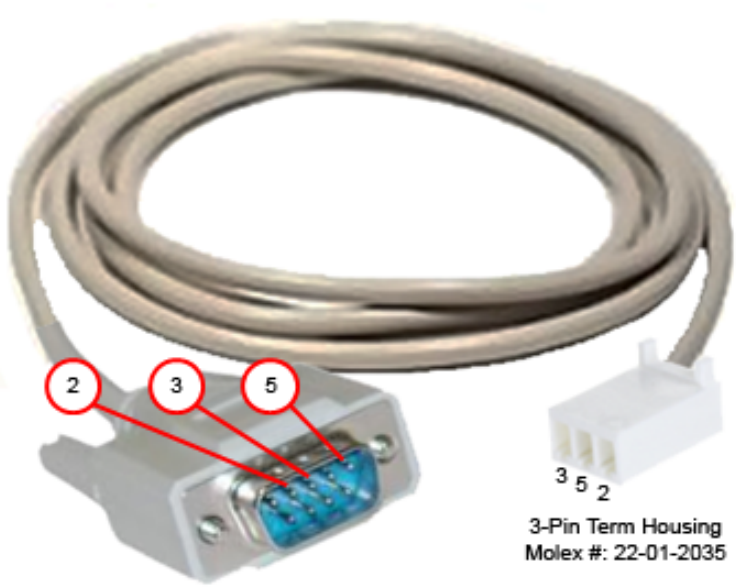
1.2 Hardware

1.2.1 Tornado VR PCIe Board with Optional Sonnet Communication Interface



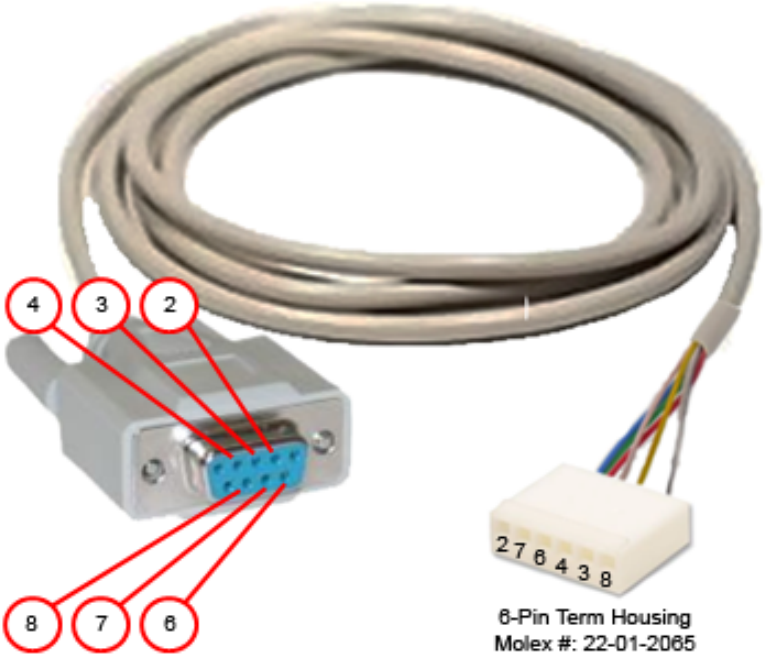
1	Optional Sonnet Communication Interface		10	HD Input Group
2	Two Vision Research RTO Input Ports		11	External Poer LED
3	Status LEDs: PCIe Link to Host (Top) PCIe Link to FPGA Status (Middle) PCIe Link to Option Board (Bottom)		12	5V Fan Power Port
4	PCIe 8x Connector		13	IIC Optional Port (12C)
5	Configuration Programming Port		14	Top of Frame Sync Out
6	Health LED		15	HD Output Group
7	Optional 12V Power Out, Fan Power		16	Optional Board Connector (Reverse Side)
8	PCIe 12V Power		17	Two RS-422; One RS-232
9	Analog Iris Control			

1.2.2 RS-232 Connector



PIN	FUNCTIONAL DESCRIPTION
2	Transmit Data
3	Receive Data
5	Ground

1.2.3 RS-422 Connector



PIN	FUNCTIONAL DESCRIPTION		PIN	FUNCTIONAL DESCRIPTION
2	Transmit Data (Positive)		6	Ground
3	Receive Data (Positive		7	Transmit Data (Negative)
5	Ground		8	Receive Data (Negative

1.3 Tornado VR PCIe Board

1.3.1 IIC Bus

The IIC Bus may be accessed either by an off-board processor (163077) or through the FPGA, detailed below. The following devices are connected to the IIC Bus:

Device: Maxim DS3502 IIC Pot

Address: 0x28

Details: The DS3502 is an electronic potentiometer whose output can be adjusted from 0V to 9V for controlling an analog device, such as an iris.

Device: Maxim MAX6642 Remote/Local Temperature Sensor

Address: 0x49

Details: The MAX6642 is an electronic thermometer that can be used to monitor the temperature of the PCB and the core temperature of the FPGA.

Device: PLX PEX8624 PCI Express Switch

Address: 0x68

Details: The PEX8624 configuration registers can be accessed at this address.

Device: XFP Module

Address: 0x50

Details: The XFP Optical Module can be accessed at this address.

1.3.2 MD Bus

The MD Bus may be accessed either by an off-board processor (163077) or through the FPGA, detailed below. The following device is connected to the MD Bus:

Device: AMCC S19237 SONET Transceiver

Address: 0x04

Details: The S19237 configuration registers can be accessed at this address.

1.3.3 PCI Express Bus

The Tornado VR PCIe Board (163078) is accessed via the PCI Express Bus. Two devices are present: the PEX8624 PCI Express Switch with Vendor ID 0x10B5 and Device ID 0x8624 and the FPGA with Vendor ID 0x12D1 and Device ID 0x0510.

1.3.3.1 PCI Memory Bank 0

1.3.3.1.1 Buffer SDRAM

Range: 0x00000000-0x01FFFFFF

Direction: Read/Write

Description: This address range contains 32MB of SDRAM used to store on-demand displayed frames, as described under Frame Hold Control/Status Register.

1.3.3.2 PCI Memory Bank 1

1.3.3.2.1 FPGA Control/Status Register

Range: 0x00000000

Direction: Read/Write

Description: This address provides control of and status for the Tornado VR PCIe Board operations.

Bits	Function
0-6	Camera Select (default 0)
7-8	not used
9	Noise Processing Enable (high true, default 0)
10	Noise Offset Bypass Enable (high true, default 0)
11	Noise Scale Bypass Enable (high true, default 0)
12-29	not used
30	ROI2 Display Select (0 = ROI1, 1 = ROI2)
31	Manual Buffer Enable (high true, default 0)

Current Camera Select values are:

Value	Camera
0	None/Camera Capture disabled (default)
8	HD Input
50	Vision Research RTO

1.3.3.2.2 Display Frame Dimensions Register

Range: 0x00000004

Direction: Read/Write

Description: When the Camera Select value in the FPGA Control Register is set to 0 or to a Generic camera type, the values placed in this register are used by the Bayer conversion logic and the HD output to determine the format of the stored frames, otherwise, the format is a function of the selected camera.

Bits	Function
0-10	Frame X size in pixels (default 1280)
11-15	not used
16-26	Frame Y size in lines (default 1024)
27	not used
28-31	Pixel Format (default 0, not used)

Current Pixel Format values are:

Value	Pixel Format
0	HD Format, YCrCb (default)
1	24 Bit RGB (out of 32 bits)
2	10 Bit /Pixel Bayer/Monochrome (out of 16bits)
3	8 Bit/Pixel Bayer/Monochrome
4	Not used
5	Not used
6	Not used

In HD Data Format, the FPGA will treat the pixel data in the transmit buffers as 20 bit per pixel HD format (even pixel Y in bits 10-19, CrCb in bits 0-9, odd pixel Y in bits 42-51, CrCb in bits 32-41, bits 20-31 & 52-63 are not used). If the Monochrome bit in the HD Control Register is also set, the CrCb data is forced to 0.

For 24 Bit RGB, the pixel data is assumed to be blue even in bits 0-7, green in 8-15, red in 16-23, blue odd in 32-39, green in 40-47, red in 48-55. Bits 24-31 & 56-63 are unused.

When 10 Bit/Pixel Bayer/Monochrome is selected, pixel data is stored in the buffer first pixel in bits 16-25, second in 0-9, third in 48-57, fourth in 32-41. Remaining bits are ignored. If the Monochrome bit in the HD Control Register is set, the pixels are treated as monochrome, otherwise, they are converted into color.

If 8 Bit/Pixel Bayer/Monochrome is selected, pixel data is stored in the buffer first pixel in bits 24-31, second in 16-23, third in 8-15, fourth in 0-7, fifth in 56-63, sixth in 48-55, seventh in 40-47, eighth in 32-39. If the Monochrome bit in the HD Control Register is set, the pixels are treated as monochrome, otherwise, they are converted into color.

Note that the Frame X size value in this register should be set to the smaller of the image's width and the HD output width.

1.3.3.2.3 Interrupt Enable Register

Range: 0x00000008

Direction: Read/Write

Description: The Tornado VR PCIe Board can be made to generate interrupts to the PCIe bus. The Interrupt Enable Register is used to select the sources of the interrupts. Its bits are defined as follows:

Bits	Function
0	DMA Read Interrupt
1	DMA Write Interrupt
2	Frame Hold/Decimation Complete
3-9	not used
10	UART 1 Rx Data Available
11	UART 1 Tx FIFO No Longer Full
12	UART 2 Rx Data Available
13	UART 2 Tx FIFO No Longer Full
14	UART 3 Rx Data Available
15	UART 3 Tx FIFO No Longer Full
16	not used
17	Capture End-of-Frame
18	HD Output Start-of-Frame
19	HD Input Start-of-Frame
20	RTO Start-of-Frame
21	PEX8624 PEX_INTA#
22	S19237 TX_RX_ALARM
23	XFP Module Interrupt
24	XFP Module RX_LOS
25	XFP Module Mod_NR
26	XFP Module Mod_Abs
27	GSPI Complete
28	SPI Complete
29	MDIO Complete
30	IIC Complete
31	IIC No Acknowledge

1.3.3.2.4 Interrupt Status Register

Range:0x0000000C

Direction: Read only

Description: Upon receiving an Tornado VR PCIe Board interrupt, the CPU should read this location to determine which interrupt has been generated. Writing the value read into the Interrupt Clear Register will clear the pending interrupts. The bits are defined as follows:

Bits	Function
0	DMA Read Interrupt
1	DMA Write Interrupt
2	Frame Hold/Decimation Complete
3-9	not used
10	UART 1 Rx Data Available
11	UART 1 Tx FIFO No Longer Full
12	UART 2 Rx Data Available
13	UART 2 Tx FIFO No Longer Full
14	UART 3 Rx Data Available
15	UART 3 Tx FIFO No Longer Full
16	not used
17	Capture End-of-Frame
18	HD Output Start-of-Frame
19	HD Input Start-of-Frame
20	RTO Start-of-Frame
21	PEX8624 PEX_INTA#
22	S19237 TX_RX_ALARM
23	XFP Module Interrupt
24	XFP Module RX_LOS
25	XFP Module Mod_NR
26	XFP Module Mod_Abs
27	GSPI Complete
28	SPI Complete
29	MDIO Complete
30	IIC Complete
31	IIC No Acknowledge

1.3.3.2.5 Interrupt Clear Register

Range: 0x0000000C

Direction: Write only

Description: After the receipt of an Tornado VR PCIe Board interrupt, the CPU must write to this register to clear any pending interrupts. Typically, the value read from the Interrupt Status will be the correct write data for this purpose. The bits are defined as follows:

Bits	Function
0	DMA Read Interrupt
1	DMA Write Interrupt
2	Frame Hold/Decimation Complete
3-10	not used
11	UART 1 Tx FIFO No Longer Full
12	not used
13	UART 2 Tx FIFO No Longer Full
14	not used
15	UART 3 Tx FIFO No Longer Full
16	not used
17	Capture End-of-Frame
18	HD Output Start-of-Frame
19	HD Input Start-of-Frame
20	RTO Start-of-Frame
21-26	not used
27	GSPI Complete
28	SPI Complete
29	MDIO Complete
30	IIC Complete
31	IIC No Acknowledge

1.3.3.2.6 Endian Register

Range:0x00000010

Direction: Read/Write

Description: This register sets the byte endianness of the Buffer SDRAM and the Register space. Default (value of 0) matches PCI Express endianness.

Bits	Function
0	Buffer SDRAM
1	Register Space

1.3.3.2.7 Frame Hold Control/Status Register

Range:0x00000014

Direction: Read/Write

Description: This register provides control and status for the Frame Hold function. Its bits are defined as follows:

Bits	Function
0	Frame Hold Enable
1	Decimation Select
2-3	Frame Hold Format
4-31	not used

Current Frame Hold Format values are:

Value	Camera
0	24 bit Unpacked xRGB (default)
1	30 bit Unpacked xRGB
2 2	4 bit Packed RGB

Setting the Frame Hold Enable bit will cause the next displayed frame to be copied into the Frame Hold Buffer, in the selected Frame Hold Format. The frame is stored in the buffer in sequential locations so that it may be copied out in a single DMA operation.

Once set, the Frame Hold Enable bit will remain set until a full frame has been copied into the buffer. Upon completion, an interrupt will be generated.

1.3.3.2.8 UART Status Register

Range:0x00000018

Direction: Read only

Description: This register provides status information for the 3 UARTs. Its bits are defined as follows:

Bits	Function
0-3	not used
4	UART 1 Rx Parity Error
5	UART 1 Rx Framing Error
6	UART 1 Rx Data Available
7	UART 1 Tx FIFO Full
8	UART 2 Rx Parity Error
9	UART 2 Rx Framing Error
10	UART 2 Rx Data Available
11	UART 2 Tx FIFO Full
12	UART 3 Rx Parity Error
13	UART 3 Rx Framing Error
14	UART 3 Rx Data Available
15	UART 3 Tx FIFO Full
16-31	not used

1.3.3.2.9 UART Baud Rate Register

Range:0x0000001C

Direction: Read/Write

Description: This register determines the Baud rates and parity of UARTs 1-3. Its bits are defined as follows:

Bits	Function
0-3	not used
4-7	UART 1 Baud Rate (default 1)
8-11	UART 2 Baud Rate (default 1)
12-15	UART 3 Baud Rate (default 1)
16-19	not used
20	UART 1 Parity Polarity (default 0 = even)
21	UART 1 Parity Enable (default 0 = none)
23	UART 2 Parity Polarity (default 0 = even)
24	UART 2 Parity Enable (default 0 = none)
26	UART 3 Parity Polarity (default 0 = even)
27	UART 3 Parity Enable (default 0 = none)
28-31	not used

Valid Baud Rate values are:

Value	Baud Rate
0	4800
1	9600
2	19200
3	38400
4	115200

1.3.3.2.10 Gennum Control Register

Range:0x00000020

Direction: Read/Write

Description: This register provides access to the Gennum parts external control pins. Under normal operating conditions this register should not need to be changed. The bits are defined as follows:

Bits	Function
0	not used
1	Channel 1 GS2972 DVB_ASI (default 0: does not support DVB-ASI)
2	Channel 1 GS2972 SMPTE_BYPASS (default 1: SMPTE mode enabled)
3	Channel 1 GS2972 IOPROC_EN/DIS (default 1: I/O Processing enabled)
4	Channel 1 GS2972 SDO_EN/DIS (default 1: SDO enabled)
5	Channel 1 GS2972 DETECT_TRS (default 1: lock to external TRS)
6	Channel 1 GS2972 STANDBY (default 0: device is enabled)
7	Channel 1 GS2972 TIM_861 (default 0: ignored)
8	Channel 1 GS2972 ANC_BLANK (default 1: pass Luma & Chroma as is)
9	Channel 1 GS2970 DVB_ASI (default 0: does not support DVB-ASI)
10	Channel 1 GS2970 SMPTE_BYPASS (read only)
11	Channel 1 GS2970 IOPROC_EN/DIS (default 1: I/O Processing enabled)
12	Channel 1 GS2970 STANDBY (default 0: device is enabled)
13	Channel 1 GS2970 SW_EN (default 0: automatic lock)
14	Channel 1 GS2970 TIM_861 (default 0: ignored)
15	Channel 1 GS2970 AUDIO_EN/DIS (default 0: audio disabled)
16	not used
17	Channel 2 GS2972 DVB_ASI (default 0: does not support DVB-ASI)
18	Channel 2 GS2972 SMPTE_BYPASS (default 1: SMPTE mode enabled)
19	Channel 2 GS2972 IOPROC_EN/DIS (default 1: I/O Processing enabled)
20	Channel 2 GS2972 SDO_EN/DIS (default 1: SDO enabled)
21	Channel 2 GS2972 DETECT_TRS (default 1: lock to external TRS)
22	Channel 2 GS2972 STANDBY (default 0: device is enabled)
23	Channel 2 GS2972 TIM_861 (default 0: ignored)
24	Channel 2 GS2972 ANC_BLANK (default 1: pass Luma & Chroma as is)
25	Channel 2 GS2970 DVB_ASI (default 0: does not support DVB-ASI)
26	Channel 2 GS2970 SMPTE_BYPASS (read only)
27	Channel 2 GS2970 IOPROC_EN/DIS (default 1: I/O Processing enabled)
28	Channel 2 GS2970 STANDBY (default 0: device is enabled)
29	Channel 2 GS2970 SW_EN (default 0: automatic lock)
30	Channel 2 GS2970 TIM_861 (default 0: ignored)
31	Channel 2 GS2970 AUDIO_EN/DIS (default 0: audio disabled)

1.3.3.2.11 Camera Status/Control

Range:0x00000024

Direction: Read/Write

Description: This register provides camera control and status.

Bits	Function
0	Trigger (output to camera)
1	Trigger2 (output to camera)
2	BMODE (output to camera)
3	Strobe (read only, from camera)
4-31	not used

1.3.3.2.12 Buffer Ready

Range:0x00000028

Direction: Write only

Description: Writing a Capture Buffer's number to this register will mark that buffer as ready for transmission.

Bits	Function
0-7	Buffer Number
8-31	not used

1.3.3.2.13 Buffer Status

Range:0x00000028

Direction: Read only

Description: This register provides Capture Buffer status for the first 28 buffers. A high in a given bit indicates that the corresponding buffer has been marked as available for transmission, either by the Capture logic or through the Buffer Ready register, but has not yet been transmitted. When a busy bit is low, the Buffer may safely be written with a new frame.

1.3.3.2.14 Buffer Numbers

Range:0x0000002C

Direction: Read only

Description: This register provides the numbers of the current Capture & Display Buffers.

Bits	Function
0-7	Capture Buffer
8-15	Display Buffer
16-31	not used

1.3.3.2.15 Buffer SDRAM Index Register

Range:0x00000034

Direction: Read/Write

Description: When accessing the Buffer SDRAM through PCI Memory Bank 2, the contents of this register are used as the upper ten bits of the SDRAM address, dividing the SDRAM into 32 32MB regions.

Bits	Function
0-9	Index
10-31	not used

1.3.3.2.16 HD Output Buffer Enable Register

Range:0x00000038

Direction: Read/Write

Description: This register sets which one of the buffers can be used for HD Output.

Bits	Function
0-7	Buffer Number
8-31	not used

1.3.3.2.17 Buffer Release

Range:0x0000003C

Direction: Write only

Description: After a buffer has been read out, write its buffer number to this location to indicate to the hardware that it is once again available for receiving capture data.

Bits	Function
0-7	Buffer Number
8-31	not used

1.3.3.2.18 Frame Number

Range:0x00000048

Direction: Read/Write

Description: This counter indicates the number of frames received from the camera.

1.3.3.2.19 Ancillary Data

Range:0x00000050-0x0000005C

Direction: Read/Write

Description: These registers hold the 16 byte Ancillary Data to be appended to received frames.

1.3.3.2.20 Clock

Range:0x00000060-0x00000068

Direction: Read/Write

Description: Write to these registers to set the clock. They must be written in address-order for their contents to be transferred to the clock. Specifically: write to the Seconds register (0x00000060) first, followed by the Minutes/Hour/Day register (0x00000064), then the Month/Year register (0x00000068). To read the current time, the registers must be read out in the same order.

The register contents are as follows:

Seconds register (0x00000060):

Bits	Function
0-3	Microseconds 1s
4-7	Microseconds 10s
8-11	Microseconds 100s
12-16	Milliseconds 1s
16-19	Milliseconds 10s
20-23	Milliseconds 100s
24-27	Seconds 1s
28-31	Seconds 10s

Minutes/Hour/Day register (0x00000064):

Bits	Function
0-3	Minutes 1s
4-7	Minutes 10s
8-11	Hour 1s
12-15	Hour 10s
16-19	Day 1s
20-23	Day 10s
24-31	Not used

Month/Year register (0x00000068):

Bits	Function
0-3	Month 1s
4-7	Month 10s
8-11	Year 1s
12-15	Year 10s
16-19	Year 100s
20-23	Year 1000s
24-31	Not used

Note that the clock runs in 24-hour format only and no attempt is made to track the calendar. That is: the day will count from 0-99 and the month and year are not counted. All values are 4 bit BCD.

1.3.3.2.21 Frame Read X Offset Register

Range:0x0000006C

Direction: Read/Write

Description: The value in this register is the byte offset for each line read out during Frame Reads.

1.3.3.2.22 HD X Offset Register

Range:0x00000070

Direction: Read/Write

Description: The value in this register is the byte offset for each line read out during HD display when a Generic camera type is selected.

1.3.3.2.23 Revision Register

Range:0x00000074

Direction: Read only

Description: This register returns the current FPGA revision.

1.3.3.2.24 Frame Rate Register

Range:0x00000078

Direction: Read only

Description: This register is the frame rate in frames per second for the currently selected input.

1.3.3.2.25 Miscellaneous Status

Range:0x0000007C

Direction: Read only

Description: This register provides miscellaneous status.

Bits	Function
0	XFP Module Tx Enable (high true)
1	CPU Board Detect (low true)
2	PEX8624 PEX_INTA# (high true)
3	S19237 TX_RX_ALARM (high true)
4	XFP Module Interrupt (high true)
5	XFP Module RX_LOS (high true)
6	XFP Module Mod_NR (high true)
7	XFP Module Mod_Abs (high true)
8	RTO 0 RX_EN (high true)
9	RTO 0 SQ_EN (high true)
10	RTO 0 EN_SD (high true)
11	RTO 0 SD (high true)
12	RTO 1 RX_EN (high true)
13	RTO 1 SQ_EN (high true)
14	RTO 1 EN_SD (high true)
15	RTO 1 SD (high true)
16-31	not used

1.3.3.2.26 Optical Module Control

Range:0x0000007C

Direction: Write only

Description: This register provides control of the optical modules (XFP & RTO).

Bits	Function
0	XFP Module Tx Enable (high true)
1-7	not used
8	RTO 0 RX_EN (high true)
9	RTO 0 SQ_EN (high true)
10	RTO 0 EN_SD (high true)
11	not used
12	RTO 1 RX_EN (high true)
13	RTO 1 SQ_EN (high true)
14	RTO 1 EN_SD (high true)
15-31	not used

1.3.3.2.27 HD Control Register

Range: 0x00000080

Direction: Read/Write

***** EXPAND 720 TO 1080 IS CURRENTLY DISABLED *****

Description: This address provides control of HD operations.

Bits	Function
0-3	System Number (default 3)
4	1080 Select (high true)
5	not used
6	Monochrome (high true)
7	Bayer 3x3 Matrix Select (high true)
8	In Clock to Out Clock Select (high true)
9	HD Loop Enable (high true)
10	HD Out Blank Enable (high true)
11	Bayer Pattern Invert (0 = first line Green-Red, 1 = first line Blue-Green)
12	Annotation Enable (high true, default 0)
13	Dual-Link Enable (high true)
14	Progressive Segmented Frame Enable (high to enable)
15	Expand 720 to 1080 Enable (high to enable)
16-25	Bayer 3x3 Threshold
26	Bayer Red/Blue Swap (high true)
27-31	not used

The System Number and 1920 Select bits set the format of the transmitted frames. Refer to SMPTE 274M and 296M for format specifics. If 1080 Select is low, 1280x720 progressive scan frames per SMPTE 296M are created. All 8 System Numbers are supported. With 1080 Select high, 1920x1080 frames per SMPTE 274M are generated. All System Numbers are fully supported. In addition, Frame Segmentation is supported for System Numbers 7 through 11 by setting the Progressive Segmented Frame Enable bit.

In normal operation frames are taken from the Buffers for transmission. This is what happens when the HD Loop Enable bit is low. Setting this bit high will disable the transmission of buffered frames and instead send whatever is being received from the HD In port. The HD Out Blank Enable bit, when set, will force the HD output to constant black.

Normally, the HD Out port is clocked by the Timing Generator, dependent on the System Number and 1920 Select bits. However, when the In Clock to Out Clock Select bit is set, the clock from the HD In port is used as the HD Out clock, regardless of the System Number and 1920 Select bits.

The Annotation Enable bit enables the display of a line of text up to 63 characters long over the displayed image. The text is white on black and can be placed anywhere on screen. By default, a 5x5 matrix is used for Bayer Pattern processing. Setting the Bayer 3x3 Matrix Select bit will enable the use of the 3x3 matrix from the original Bayer conversion.

When the Dual-Link Enable bit is set, the luminance is output on the primary HD-SDI link and the chrominance is output on the secondary link per SMPTE 372M. Otherwise, the luminance and chrominance are multiplexed on the primary link per SMPTE 292M.

1.3.3.2.28 HD Status Register

Range: 0x00000084

Direction: Read only

Description: This address provides HD status. For more information on the incoming video, refer to the Gennum GS2970 data sheet.

Bits	Function
0-8	not used
9	HD Input Format (high = 1920x1080, low = 1280x720)
10	not used
11-18	HD Input VPID
19	HD Input Interlaced (high true)
20-31	not used

1.3.3.2.29 HD Output Dimensions

Range: 0x00000090

Direction: Read only

Description: This location returns the HD output dimensions. The bits are defined as follows:

Bits	Function
0-10	Width in pixels
11-15	not used
16-26	Height in lines
27-29	not used
30	Progressive Segmented Frame
31	Interlace

1.3.3.2.30 Frame Offset Register

Range: 0x0000009C

Direction: Read/Write

Description: This 13 bit register sets the offset in lines from the start of the buffer at which the display will begin. Note that for Bayer conversion to work properly the offset must be a multiple of 2. The default value is 0.

1.3.3.2.31 Genlock Trigger

Range: 0x000000A0

Direction: Write only

Description: Writing a 1 to the Trigger bit in this register will force the HD Output to synchronize to the next Top-of-Frame event on the HD Input. Writing a 1 to the Genlock Now bit will force the HD Output to start a new frame immediately.

Bits	Function
0	Trigger bit
1-15	not used
16	Genlock Now bit
17-31	not used

1.3.3.2.32 Annotation Origin Register

Range: 0x000000A4

Direction: Read/Write

Description: This register sets the display origin for Frame Annotation. A First Pixel value of 0 corresponds to the leftmost position on the screen, and a First Line of 0 is at the top of the screen.

Bits	Function
0-10	First Pixel
11-15	not used
16-26	First Line
27-31	not used

1.3.3.2.33 Annotation Width Register

Range: 0x000000A8

Direction: Read/Write

Description: This register sets the number of characters to be displayed by Frame Annotation, up to 63. It also sets the character magnification. Valid values for the magnification are 0-3, corresponding to magnification of 1, 2, 4, or 8 times, respectively.

Bits	Function
0-5	Number of characters
6-7	not used
8-9	Character Magnification
10-31	not used

1.3.3.2.34 Timing Generator Control Register

Range: 0x000000AC

Direction: Read/Write

Description: This register can be used to control the Video/Audio Timing Generator. Its bits are defined as follows:

Bits	Function
0-5	Video Standard Select (default 0)
6	not used
7	Video Standard Enable (default 0)
8-10	Audio Sample Rate Select (default 3)
11	Genlock Select (default 0 = HD-SDI In 1, 1 = HD-SDI In 2)
12-29	not used
30	Timing Generator REF_LOST (read only)
31	Timing Generator LOCK_LOST (read only)

Refer to the Gennum GS4911B data sheet for valid Video Standard Select and Audio Sample Rate Select values.

When the Video Standard Enable bit (bit 7) is low, the Video Standard is set according to the HD Control Register System Number and 1920 Select bits. When high, the Video Standard Select bits are used instead.

Genlock is currently disabled.

1.3.3.2.35 RGB Transform Registers

Range: 0x000000B0-0x000000B8

Direction: Read/Write

Description: In the display pixel path, an optional transform can be perform on the red, green, and blue pixel values before they are presented to the Gamma Tables. The 3 registers in this address range hold the coefficients used in the transform as follows:

Address 0x000000B0:

Bits	Function
0-9	A13
10-19	A12
20-29	A11
30	not used
31	Red Enable (high true, default low)

Address 0x000000B4:

Bits	Function
0-9	A23
10-19	A22
20-29	A21
30	not used
31	Green Enable (high true, default low)

Address 0x000000B8:

Bits	Function
0-9	A33
10-19	A32
20-29	A31
30	not used
31	Blue Enable (high true, default low)

Each coefficient is a 10 bit two's-complement value in the range of -1.000 to +0.996 (0x200 to 0x1FF). The equations used in the transform are:

RO = RI*A11 + GI*A12 + BI*A13

GO = RI*A21 + GI*A22 + BI*A23

BO = RI*A31 + GI*A32 + BI*A33

Note that, by default, the transforms are disabled and the inputs are passed directly to the outputs. The enable bit must be set high to enable the transform for the corresponding color.

1.3.3.2.36 SPI Interface Register

Range: 0x000000C0

Direction: Read/Write

Description: Writing to this register will initiate an access to the SPI device (Atmel AT25640A) attached to the FPGA. Reading will return the SPI Interface Busy status and the most recently read data. Completion of the transaction can be determined by monitoring the Busy bit or by using the SPI Complete interrupt.

Bits	Function
0-7	READ/WRITE/RDSR/WRSR Data
8-23	READ/WRITE Address
24-25	Instruction Select
26	READ/WRITE/RDSR/WRSR Direction (high to write)
27	Busy (read only, high true)
28-31	not used

The Instruction Select bits are encoded as follows:

Value	Instruction
0	RDSR/WRSR (Read/Write Status Register)
1	WREN (Set Write Enable Latch)
2	WRDI (Reset Write Enable Latch)
3	READ/WRITE (Read/Write Data Memory Array)

1.3.3.2.37 MDIO Interface Register

Range: 0x000000C4

Direction: Read/Write

Description: Writing to this register will initiate an access to the MDIO device (AMCC S19237 SONET Transceiver, PHY Address 4) attached to the FPGA. Reading will return the MDIO Interface Busy status and the most recently read data. Completion of the transaction can be determined by monitoring the Busy bit or by using the MDIO Complete interrupt.

Bits	Function
0-15	Read/Write Data
16-20	Register Address
21-25	PHY Address
26	Direction (high to write)
27	Busy (read only, high true)
28-31	not used

1.3.3.2.38 IIC Interface Register

Range: 0x000000C8

Direction: Read/Write

Description: Writing to this register will initiate an access to the IIC devices attached to the FPGA (see above). Reading will return the IIC Interface Busy status and the most recently read data. Completion of the transaction can be determined by monitoring the Busy bit or by using the IIC Complete interrupt.

If the addressed device does not respond to the requested access, an IIC No Acknowledge interrupt can be generated and the No Acknowledge bit will be set. The No Acknowledge bit will be cleared by writing to this register.

Bits	Function
0-7	Read/Write Data
8	Direction (high to write)
9-15	Address
16-23	Register Address
24	Send Register Address (high true)
25	Busy (read only, high true)
26	No Acknowledge (read only, high true)
27-31	not used

1.3.3.2.39 Gennum Interface Register

Range: 0x000000CC

Direction: Read/Write

Description: Writing to this register will initiate an access to the Gennum devices attached to the FPGA. Reading will return the most recently read data. Completion of the transaction can be determined by monitoring the Busy bit or by using the GSPI Complete interrupt.

Bits	Function
0-15	Read/Write Data
16-27	Register Address
28-30	Device Address
31	Direction (high to write)

The Gennum Device Addresses are as follows:

Value	Device
0	Primary GS2970 HD-SDI Input
1	Primary GS2972 HD-SDI Output
2	Secondary GS2970 HD-SDI Input
3	Secondary GS2972 HD-SDI Output
4	GS4911B HD-SDI Output Timing Generator

1.3.3.2.40 Gennum Interface Busy Register

Range: 0x000000D0

Direction: Read only

Description: Reading this register will return the Gennum Interface Busy status.

Bits	Function
0	Busy (high true)
1-31	not used

1.3.3.2.41 DMA Enable Register

Range: 0x000000D4

Direction: Read/Write

Description: Setting the DMA Enable bit in this register will initiate the DMA accesses defined in the DMA Descriptor RAM. The bit will remain high until the DMAs have completed. Clearing the bit will abort any DMA in progress.

Bits	Function
0	DMA Enable (high true)
1-15	not used
16-25	Descriptor Number (read only)
26-31	not used

1.3.3.2.42 DMA Trigger Register

Range: 0x000000D8

Direction: Read/Write

Description: When the Trigger on Event bit is set in a DMA Descriptor, processing of the descriptor will be delayed until the event specified in this register has occurred.

Bits	Function
0-1	Trigger Type
2-15	not used
16-27	Delay in 4µs. increments
28-31	not used

Trigger Types are as follows:

Value	Device
0	EOF
1	EOF with delay
2	SOF
3	SOF with delay

1.3.3.2.43 RTO Packet Error Register

Range: 0x000000DC

Direction: Read only

Description: This register returns the counts of RTO packet errors. Reading it will reset the counts.

Bits	Function
0-15	ROI0 Packet Error Count
16-31	ROI1 Packet Error Count

1.3.3.2.44 RTO ROI1 Data Register

Range: 0x000000E0

Direction: Read only

Description: This register provides data extracted from the RTO Frame Start Packet for ROI1. For details, refer to the Vision Research documentation.

Bits	Function
0-7	Format
8-15	Frame Count
16-31	Line Size

1.3.3.2.45 RTO ROI1 Image Size Register

Range: 0x000000E4

Direction: Read only

Description: This 32 bit register returns the image size in bytes per channel extracted from the RTO Frame Start Packet for ROI1. For details, refer to the Vision Research documentation.

1.3.3.2.46 RTO ROI1 Dimensions Register

Range: 0x000000E8

Direction: Read/Write

Description: This register sets the dimensions of images coming from the Vision Research camera for ROI1. See note in RTO ROI0 Dimensions Register.

Bits	Function
0-15	Frame Width in pixels (range 64-4095)
16-31	Frame Height in lines (range 2-4095)

1.3.3.2.47 RTO ROI0 Data Register

Range: 0x000000EC

Direction: Read only

Description: This register provides data extracted from the RTO Frame Start Packet for ROI0. For details, refer to the Vision Research documentation.

Bits	Function
0-7	Format
8-15	Frame Count
16-31	Line Size

1.3.3.2.48 RTO ROI0 Image Size Register

Range: 0x000000F0

Direction: Read only

Description: This 32 bit register returns the image size in bytes per channel extracted from the RTO Frame Start Packet for ROI0. For details, refer to the Vision Research documentation.

1.3.3.2.49 RTO Channel Number Register

Range: 0x000000F4

Direction: Read only

Description: This location provides the logical channel numbers from the Vision Research camera.

Bits	Function
0-15	not used
16-23	RTO0 Channel Number from header
24-27	RTO1 Channel Number from header
28-31	not used

1.3.3.2.50 RTO ROI0 Dimensions Register

Range: 0x000000F8

Direction: Read/Write

Description: This register sets the dimensions of images coming from the Vision Research camera for ROI0. Note that for proper operation, for V7 camera the number of lines must be a multiple of 8 and the number of pixels must be a multiple of 64 for 8bpp Pixel Format or 32 for other formats, and for DS10/440 the number of lines must be even and the number of pixels must be a multiple of 192 for 8bpp Pixel Format or 96 for other formats.

Bits	Function
0-15	Frame Width in pixels (range 64-4095)
16-31	Frame Height in lines (range 2-4095)

1.3.3.2.51 RTO Control Register

Range: 0x000000FC

Direction: Read/Write

Description: This register provides control of the formatting of the data coming from the Vision Research camera. For details, refer to the Vision Research documentation.

Writing to this register will reset the RTO interface.

Bits	Function
0-2	Pixel Format
3	not used
4	Twelve Channels per ROI (low = 6 channels, high = 12 channels)
5	not used
6	ROI Orientation (0 = Vertical, 1 = Horizontal)
7	ROI 1 Enable (high to enable)
8	not used
9	Block 1 Disable (RTO 0 Channels 8-11, default low, high to disable)
10	Block 2 Disable (RTO 1 Channels 0-7, default low, high to disable)
11	Block 3 Disable (RTO 1 Channels 8-11, default low, high to disable)
12	V7 Select (0 = other camera, 1 = V7)
13-15	not used
16-17	PRBS Select (see GTX documentation)
18	PRBS Enable
19	not used
20-23	Channel Number Index
24-31	not used

The Pixel Format bits are encoded as follows:

Value	Format
0	8 bpp
1	10 bpp
2	12 bpp
3	Raw
4	14 bpp (currently not supported)
5	16 bpp (currently not supported)
6	Cinestream10bpp
7	Cinestream 8bpp

1.3.3.2.52 Frame Hold Buffer Offset

Range: 0x00000100

Direction: Read/Write

Description: This register sets the offset in the Buffer SDRAM for the Frame Hold Buffer. Its bits are defined as follows:

Bits	Function
0-19	not used
20-29	Offset
30-31	not used

Note that the offset is on 1MB boundaries. By default, the Frame Hold Buffer is at offset 0x3A000000 and is 32MB in size.

1.3.3.2.53 Noise Processing Offset Buffer Offset

Range: 0x00000104

Direction: Read/Write

Description: This register sets the offset in the Buffer SDRAM for the Noise Processing Offset Buffer. Its bits are defined as follows:

Bits	Function
0-19	not used
20-29	Offset
30-31	not used

Note that the offset is on 1MB boundaries. By default, the Noise Processing Offset Buffer is at offset 0x3C000000 and is 32MB in size.

1.3.3.2.54 Noise Processing Scale Buffer Offset

Range: 0x00000108

Direction: Read/Write

Description: This register sets the offset in the Buffer SDRAM for the Noise Processing Scale Buffer. Its bits are defined as follows:

Bits	Function
0-19	not used
20-29	Offset
30-31	not used

Note that the offset is on 1MB boundaries. By default, the Noise Processing Scale Buffer is at offset 0x3E000000 and is 32MB in size.

1.3.3.2.55 UARTS

Range: 0x00001010-0x0000103C

Direction: Read/Write

Description: The Tx & Rx FIFOs of the three UARTs are addressed in this range as follows:

Address	UART
0x00001010	UART 1
0x00001020	UART 2
0x00001030	UART 3

Each UART has a 16 entry transmit FIFO and a 16 entry receive FIFO.

Bits	Function
0-7	Data
8-31	not used

1.3.3.2.56 RGB Gamma RAM

Range: 0x00020000-0x00020FFC

Direction: Read/Write

Description: The RGB Gamma RAM provides a means for adjusting the individual color outputs from the Bayer convertor. By default, no adjustment is applied. Each color has its own 1024 by 10 bit RAM. They are located as follows:

Bits	Function
0-9	Blue
10-19	Green
20-29	Red
30-31	not used

1.3.3.2.57 Annotation Font RAM

Range: 0x00021000-0x000217FC

Direction: Read/Write

Description: The font used in Frame Annotation is stored in this RAM. There are 128 characters of 8 pixels by 16 lines. Since this is a 32 bit wide RAM, 4 lines of pixels are read and written at a time, as follows:

Bits	Function
0	Fourth line, last pixel
1	Fourth line, seventh pixel
2	Fourth line, sixth pixel
3	Fourth line, fifth pixel
4	Fourth line, fourth pixel
5	Fourth line, third pixel
6	Fourth line, second pixel
7	Fourth line, first pixel
8	Third line, last pixel
-	---
15	Third line, first pixel
16	Second line, last pixel
-	---
23	Second line, first pixel
24	First line, last pixel
-	---
31	First line, first pixel

Address bits 2-3 select the lines/pixels within each character and bits 4-10 select the character.

1.3.3.2.58 Buffer Table RAM

Range: 0x00021800-0x00021BFC

Direction: Read/Write

Description: This RAM holds the starting offset for the Capture/Display Buffers. Up to 256 buffers can be defined. Buffers must be a minimum of 4KB in size to a maximum of 32MB, located on 4KB boundaries. Each 32 bit location defines a single buffer, as follows:

Bits	Function
0-11	not used
12-29	Buffer Start Offset
30	Last Buffer Flag (high true)
31	not used

Set the Last Buffer Flag for the final buffer in the sequence, clear it for all others.

By default, the 1GB of SDRAM is divided into 28 32MB Capture/Display Buffers, plus four other buffers, addressed as follows:

Offset	Function
0x00000000	Capture/Display Buffer 0
0x02000000	Capture/Display Buffer 1
0x04000000	Capture/Display Buffers 2-25
0x34000000	Capture/Display Buffer 26
0x36000000	Capture/Display Buffer 27 (Last Buffer)
0x38000000	Unassigned Memory
0x3A000000	Frame Hold Buffer
0x3C000000	Noise Processing Offset Buffer
0x3E000000	Noise Processing Scale Buffer

The highest 2 buffers are 32MB used to hold per-pixel values for Noise Processing. The Offset and Scale values are 16 bits per pixel. The Frame Hold Buffer is used to store on-demand displayed frames, as described under Frame Hold Control/Status Register and is 32MB in size.

The number of buffers and their locations can be redefined using the Buffer Table RAM and the Frame Hold Buffer Offset, Noise Processing Offset Buffer Offset and Noise Processing Scale Buffer Offset registers.

1.3.3.2.59 Annotation Text RAM

Range: 0x00024000-0x00027FFC

Direction: Read/Write

Description: The text to be displayed by Frame Annotation is stored in this RAM. It consists of 28 (one per Buffer SDRAM buffer) text buffers of 64 characters each. Since this is a 32 bit wide memory, 4 characters must be read or written at a time, as follows:

Bits	Function
0-6	Fourth Character
7	not used
8-14	Third Character
15	not used
16-22	Second Character
23	not used
24-30	First Character
31	not used

Address bits 2-5 select the characters within each buffer and bits 6-10 select the buffer.

1.3.3.2.60 DMA Descriptor RAM

Range: 0x00030000-0x0003FFFC

Direction: Read/Write

Description: This RAM holds the 1024 DMA Descriptors. Each descriptor is 128 bits long, defined as follows:

Offset 0:

Bits	Function
0	Last Flag (low true)
1	Interrupt Flag (high true)
2-31	PCIe Address bits 2-31

Offset 1:

Bits	Function
0-31	PCIe Address bits 32-63

Offset 2:

Bits	Function
0	Direction (0 = from PCIe to SDRAM, 1 = from SDRAM to PCIe)
1	Loop Enable (high true)
2-31	Length of Transfer in DWORDS (DWORD = 4 bytes)

Offset 3:

Bits	Function
0-1	not used
2-29	SDRAM Start Address
30	Trigger on Event (high true)
31	not used

When a DMA is enabled by setting the DMA Enable bit in the DMA Enable Register, DMA transfers are performed starting with the first descriptor (DMA Descriptor RAM offset 0) and continuing until a descriptor with the Last Flag zeroed is completed. If the Last Flag and Loop Enable are both true, DMA resumes at the first descriptor, but if Loop Enable is cleared, DMA stops. Data is transferred to PCIe Address from the SDRAM starting at the SDRAM Start Address for Length DWORDs. For each descriptor with the Interrupt Flag set, a DMA Interrupt will be generated upon completion of the transfer. If a descriptor has the Trigger on Event flag set, processing of the descriptor will not begin until the event specified by the DMA Trigger Register has occurred.

1.3.3.3 PCI Memory Bank 2

1.3.3.3.1 Indexed Buffer SDRAM

Range: 0x00000000-0x01FFFFFF

Direction: Read/Write

Description: The Buffer SDRAM as described above can be accessed in this bank as 32 32MB regions with the 30 bit address being formed by the concatenation of the contents of the Buffer SDRAM Index Register and PCI address bits 0-24.

1.3.4 Frame Header

Frames are stored in the Buffer SDRAM preceded by a 128 byte header. This header appears at offset 0 of each buffer immediately followed by the frame's pixel data and is used to identify the contents of the frame. Included is the Frame Start Packet sent with each RTO frame, which is left undefined in HD frames, plus formatting information required by the display hardware. Any images loaded by the host require a properly formatted header for correct display.

The contents of the header are as follows (offsets are in DWs):

Offset 0:

Bits	Function
0-15	RTO Image Size bits 16-31
16-23	RTO Frame Count
24-31	RTO Format

Offset 1:

Bits	Function
0-15	RTO Line Size
16-31	RTO Image Size bits 0-15

Offset 2:

Bits	Function
0-31	RTO Time Stamp bits 32-63

Offset 3:

Bits	Function
0-31	RTO Time Stamp bits 0-31

Offset 4:

Bits	Function
0-31	RTO Range Data bits 96-127

Offset 5:

Bits	Function
0-31	RTO Range Data bits 64-95

Offset 6:

Bits	Function
0-31	RTO Range Data bits 32-63

Offset 7:

Bits	Function
0-31	RTO Range Data bits 0-31

Offset 8:

Bits	Function
0-15	not defined
16-31	RTO Reserved

Offset 9-19:

Bits	Function
0-31	not defined

Offset 20:

Bits	Function
0-15	ROI2 Line Span in bytes
16-29	not defined

Offset 21:

Bits	Function
0-15	ROI2 Width in pixels
16-31	ROI2 Height in lines

Offset 22:

Bits	Function
0-15	Frame Line Span in bytes
16-19	Pixel Format (see below)
20-29	not defined
30	ROI2 Enabled
31	ROI Orientation (0 = Vertical, 1 = Horizontal)

Offset 23:

Bits	Function
0-15	Frame Width in pixels
16-31	Frame Height in lines

Offset 24:

Bits	Function
0-31	Frame Number

Offset 25:

Bits	Function
0-3	RTC month 1s
4-7	RTC month 10s
8-11	RTC year 1s
12-15	RTC year 10s
16-19	RTC year 100s
20-23	RTC year 1000s
24-31	not defined

Offset 26:

Bits	Function
0-3	RTC minute 1s
4-7	RTC minute 10s
8-11	RTC hour 1s
12-15	RTC hour 10s
16-19	RTC day 1s
20-23	RTC day 10s
24-31	not defined

Offset 27:

Bits	Function
0-3	RTC microseconds 1s
4-7	RTC microseconds 10s
8-11	RTC microseconds 100s
12-15	RTC milliseconds 1s
16-19	RTC milliseconds 10s
20-23	RTC milliseconds 100s
24-27	RTC seconds 1s
28-31	RTC seconds 10s

Offset 28:

Bits	Function
0-31	Ancillary Data bits 96-127

Offset 29:

Bits	Function
0-31	Ancillary Data bits 64-95

Offset 30:

Bits	Function
0-31	Ancillary Data bits 32-63

Offset 31:

Bits	Function
0-31	Ancillary Data bits 0-31

Current Pixel Format values are:

Value Pixel Format
0 HD Format, YCrCb (default)
1 24 Bit RGB (out of 32 bits)
2 10 Bit /Pixel Bayer/Monochrome (out of 16 bits)
3 8 Bit/Pixel Bayer/Monochrome
4 RTO Raw
5 14 Bit CMYG (out of 16 bits, not supported)
6 10 Bit CMYG (out of 16 bits, not supported)
7 12 Bit /Pixel Bayer/Monochrome (out of 16 bits)
8 14 Bit /Pixel Bayer/Monochrome
9 16 Bit /Pixel Bayer/Monochrome
10 Cinestream (10 of 16 bits)
11 Cinestream 8Bit/Pixel

www.visionresearch.com

Vision Research - Corporate Headquarters
100 Dey Road
Wayne, New Jersey 07470
USA
Ph: +1.973.696.4500
Toll Free: 800.737.6588
Fax: +1.973.696.0560

Vision Research - Florida Office
1002 Monterey Commons, Suite 200
Stuart, Florida 34997
USA
Ph: +1.772.286.7000
Fax: +1.772.286.6206

Vision Research Ltd. - UK
Suite F8, Bedford i-lab
Priory Business Park
Stannard Way, Bedford
MK44 3RZ, United Kingdom
Ph: +44 1234 834 850
Fax: +44 1234 834 851

Vision Research Japan
Sunroad Square Showa 203, 271-5
Shinzaike-2-chome, Hiraoka-cho,
Kakagawa-city, Hyogo, 675-0101
Japan
Ph: +81.794.56.0770
Fax: +81.794.56.0771

Vision Research Asia
Ametek Singapore Pte Ltd
No. 43 Changi South Avenue 2, #04-01
Singapore 486164
Ph: +65 6505 9034
Fax: +1.973.696.0560

Vision Resaerch - Romania
75 Icoanei Street
Bucharest, Romania
Ph: +021.210.8586